DVB-T/H Modulator Core V2.1

Product Brief (June 2019 - Rev B)

Features

ETSI, DVB-T/H (EN 300 744 V1.5.1)
Compliant baseband transmitter for Digital Terrestrial Television

- **The MVD modulator cores can be delivered with an Intermediate Frequency output or a RF output when using Analog Devices or Maxim RF DACs (see separate datasheet, available on request)**
- **Drop-in module for Spartan-6™, Virtex-6™, Artix-7™, Kintex-7™ and Virtex-7™ FPGAs**
- **Single clock (up to 150 MHz)**
- **Robust SPI input (discarding incorrect input packets)**
- **PCR re-stamping**
- **Single channel, supports hierarchical transmission**
- **Configurable Convolutional Rate**
- **Configurable in-depth interleaving for DVB-H**
- **Programmable QPSK, 16-QAM and 64-QAM Symbol Mapping**
- **Configurable support for 2k, 8k and 4k (DVB-H) OFDM modes**
- **Programmable Guard Interval (1/4, 1/8, 1/16, 1/32)**
- **Supports variable channel width 5MHz to 8MHz**
- **Intermediate frequency output for single DAC (14 bits) or baseband outputs (2 x 16 bits)**
- **Single / multi channel**
- **Fully synthesizable RTL VHDL design (not delivered) for easy customization**
- **Design delivered as Netlist**
- **MER > 42dB**
- **Carrier Suppression > 45dB**

Applications

The MVD DVB-T/H modulator may be used in applications related to terrestrial transmission, typically at the head end.

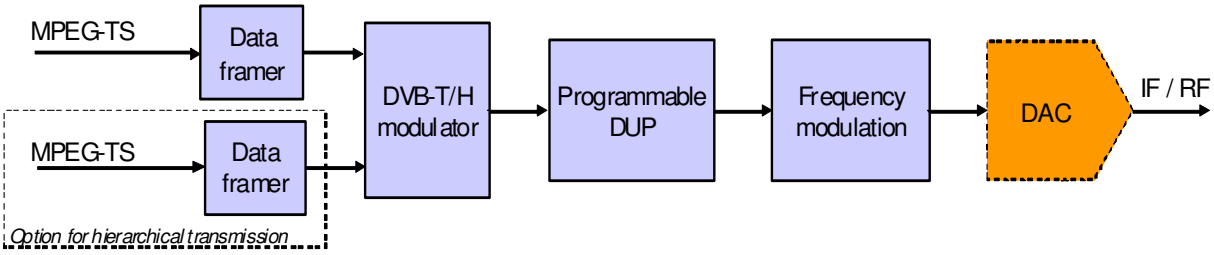
Description

The MVD DVB-T/H modulator is a drop-in module that includes the following functions :

- **Input data framer from DVB-SPI source (MPEG-TS flow)**
- **DVB-T/H modulator (Energy dispersal, Reed Solomon encoder, Convolutional interleaver, FEC convolution encoder, Inner interleaver, QPSK/QAM symbol mapper, Framer with pilots & TPS inserter, IFFT and guard interval insertion)**
- **Flexible Digital Upsampler**
- **Modulator for IF output**
- **Output for simple DAC (14 bits) or baseband outputs (2x16bits)**

Companion cores

- **ASI receiver core**
- **DVB remultiplexer core**
- **Serial Interface for CPU configuration**
- **I2C Slave Interface core**



Resource Utilization

The core configuration may be set by conditional synthesis. Typical configuration with CPU interface and without hirerchical transmission option.

	Slices	LUTs	BRAMs (18k)	Mults/DSP48	BUFG	Deliverables :
Series-6	**1900**	**6500**	**46**	**29**	**2**	- **Datasheet** - **Netlist for core generation**
Series-7	**1900**	**6500**	**43**	**29**	**2**	

Ordering information and related cores

Parameters	Designation
Fixed	**MVD_DVBTH_FIXED_NET**
CPU programmable	**MVD_DVBTH_CPU_NET**
CPU programmable + Hierarchy	**MVD_DVBTH_CPU_HIERARCHY_NET**

VHDL source code : can be delivered as an option under NDA and other specific clauses

Complementary cores : DVB-T/H for AD9789 DAC, Upconverter for AD9739 DAC or MAX5881 DAC, contact us. For a multi-channel application, we recommend to use the AD9789 for 4 adjacent channels, or we recommend to use the AD9739 DAC or the MAX5881 DAC for more than 4 channels, or for non adjacent channels.

Related cores : Cable Modulator J83B, DVB-S, DVB-C, DVB Remultiplexer and/or ASI Receiver cores contact us at *info_cores@mvd-fpga.com*

Documentation and support : Datasheet and user's guide. In addition MVD can provide on site or remote coaching.